What is claimed is:

1. A semiconductor device comprising:

a first insulating film formed over a semiconductor substrate;

capacitor constructed by forming a lower electrode, a dielectric film, and an upper electrode sequentially on the first insulating film;

a first capacitor protection insulating film covering the dielectric film and the upper electrode;

a second capacitor protection insulating film formed on the first capacitor protection insulating film; and

a second insulating film formed on the second capacitor protection insulating film;

wherein an amount of carbon contained in the second capacitor protection insulating film is larger than an amount of carbon contained in the second insulating film.

2. A semiconductor device according to claim 1, wherein the second capacitor protection insulating film is a silicon oxide film.

3. A semiconductor device according to claim 1, wherein the second insulating film is a silicon oxide film.

4. A semiconductor device according to claim 1, wherein the first capacitor protection insulating film is made of any one of alumina, PLZT, PZT, titanium oxide, aluminum nitride, silicon nitride, and silicon nitride oxide.

5. A semiconductor device according to claim 1, wherein the dielectric film is made of any one of PZT material and bismuth material.

6. A semiconductor device according to claim 1, wherein a hole reaching the upper electrode is formed in the first capacitor protection insulating film, the second capacitor protection insulating film, and the second insulating film, and

a wiring that is electrically connected to the upper electrode via the hole is formed on the second insulating film.

7. A semiconductor device manufacturing method comprising the steps of:

forming a first insulating film over a semiconductor substrate;

forming a first conductive film, a ferroelectric film, and a second conductive film sequentially on the first insulating film;

forming an upper electrode of a capacitor by patterning the second conductive film;

forming a dielectric film of the capacitor by patterning the ferroelectric film;

forming a lower electrode of the capacitor by patterning the first conductive film;

forming a first capacitor protection insulating film covering the dielectric film and the upper electrode;

forming a second capacitor protection insulating

film, which covers the first capacitor protection insulating film, by a chemical vapor deposition method in a state that a bias voltage is not applied to the semiconductor substrate; and

forming a second insulating film on the second capacitor protection insulating film by the chemical vapor deposition method in a state that the bias voltage is applied to the semiconductor substrate.

8. A semiconductor device manufacturing method according to claim 7, wherein the step of forming the first capacitor protection insulating film is carried out in the state that a bias voltage is not applied to the semiconductor substrate.

9. A semiconductor device manufacturing method according to claim 7, wherein the step of forming the second capacitor protection insulating film is carried out at a higher pressure than the step of forming the second insulating film.

10. A semiconductor device manufacturing method according to claim 7, wherein a plasma density in the step of forming the second capacitor protection insulating film is lower than the plasma density in the step of forming the second insulating film.

11. A semiconductor device manufacturing method according to claim 7, wherein the step of forming the second capacitor protection insulating film is carried out by a chemical vapor deposition method using a

reaction gas containing TEOS.

12. A semiconductor device manufacturing method according to claim 7, wherein the step of forming the second insulating film is carried out by a chemical vapor deposition method using a reaction gas containing any one of SiH_4, Si_2H_6, Si_3H_8, and $SiCl_4$.

13. A semiconductor device manufacturing method according to claim 12, wherein, in the step of forming the second insulating film, a gas containing any one of fluorine, phosphorus, and boron is added to the reaction gas.

14. A semiconductor device manufacturing method according to claim 7, wherein the step of forming the second capacitor protection insulating film includes the step of executing a hydrating process by heating the second capacitor protection insulating film.

15. A semiconductor device manufacturing method according to claim 7, wherein the step of forming the second capacitor protection insulating film includes the step of improving a film quality by exposing the second capacitor protection insulating film to a plasma atmosphere containing N (nitrogen).

16. A semiconductor device manufacturing method according to claim 7, wherein the step of forming the second insulating film includes the step of improving a film quality by exposing the second insulating film to a plasma atmosphere containing N (nitrogen).

17. A semiconductor device manufacturing method according to claim 7, wherein the step of forming the first capacitor protection insulating film includes the steps of,

forming a lower protection insulating film, which covers the dielectric film and the upper electrode, on the first conductive film,

patterning the lower protection insulating film to leave on at least the dielectric film and the upper electrode, and

forming an upper protection insulating film on the first insulating film and the lower protection insulating film, whereby the upper protection insulating film and the lower protection insulating film are applied as the first capacitor protection insulating film.

18. A semiconductor device manufacturing method according to claim 7, wherein the capacitor is formed in plural, and a total film thickness of the first capacitor protection insulating film and the second capacitor protection insulating film is set smaller than half of a minimum interval among plural upper electrodes.

19. A semiconductor device manufacturing method according to claim 7, wherein a film thickness of the second insulating film is set thicker than a total film thickness of the lower electrode, the dielectric film, and the upper electrode and is set thinner than a film thickness that is obtained by adding 1 μm to the total

film thickness.

20. A semiconductor device manufacturing method according to claim 7, wherein the step of forming the second insulating film includes the steps of,

forming a third insulating film on the second insulating film, and

planarizing surfaces of the second insulating film and the third insulating film by polishing.